IJMTARC – VOLUME – IV – ISSUE - 16 - DEC 2016 ISSN: 2320-1363

Low-Power Programmable PRPG with Test Compression Capabilities

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Abstract: Common binary arithmetic operations such as addition/subtraction and multiplication suffer from O(n) carry propagation delay where n is the number of digits. Carry lookahead helps to improve the propagation delay to O(log n), but is bounded to a small number of digits due to the complexity of the circuit. A carry-free arithmetic operation can be achieved using a higher radix number system such as Quarternary Signed Digit (QSD). In QSD, each digit can be represented by a number from -3 to 3. This number system allows multiple representations of any integer. By exploiting this feature, we can design an adder without ripple carry. The implementation of quarternary addition and multiplication results in a fix delay independent of the number of digits.Operations on a large number of digits such as 64, 128, or more, can be implemented with constant delay and less complexity.This paper focuses on the implementation of quarternary addition and multiplication. Results are verified and the performance is shown to be consistent with the constant delay model

1INTRODUCTION

Arithmetic operations are widely used and play important roles in various digital systems such as computers and signal processors. QSD number representation has attracted the interest of many researchers. Additionally, recent advances in technologies for integrated circuits make large scale arithmetic circuits suitable for VLSI implementation. However, arithmetic operations still suffer from known problems including limited number of bits, propagation time delay, and circuit complexity. In this paper, we propose a high speed QSD arithmetic logic unit which is capable of carry free addition, borrow free subtraction, up-down count and multiply operations. The QSD addition/subtraction operation employs a fixed number of minterms for any operand size. The multiplier is composed of partial product generators and adders. For convenience of testing and to verify results, we choose to

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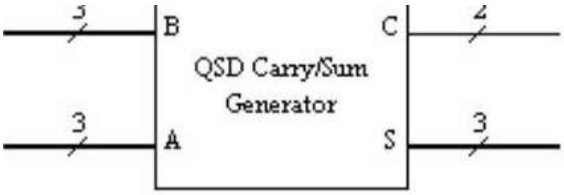
implement the units using a programmable logic device. This paper is organized as follows. the quaternary signed digit (QSD) number. The adder/subtractor and multiplier design are detailed, respectively. presents results and performance.

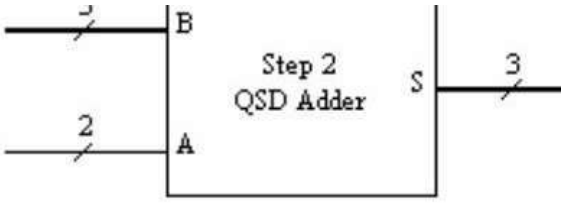
2. Adder/Subtract or Design

Addition is the most important arithmetic operation in digital computation. A carry-free addition is highly desirable as the number of digits becomes large. We can achieve carry-free addition by exploiting the redundancy of QSD numbers and the QSD addition. The redundancy allows multiple representations of any integer quantity i.e., 610=12QSD=22QSD .

INPUT				OUTPUT		
QSD		Binary		Decimal	QSD	Binary
A_i	B_i	A_i	B_i	Sum	S_i	S_i
1	2	01	010	3	3	111
1	1	01	001	2	2	010
0	2	00	010	2	2	010
0	1	00	001	1	1	001
1	0	01	000	1	1	001
-1	2	11	010	1	1	001
0	0	00	000	0	0	000
1	-1	01	111	0	0	000
-1	1	11	001	0	0	000
0	-1	00	111	-1	-1	111
-1	0	11	000	-1	-1	111
1	-2	01	110	-1	-1	111
-1	-1	11	111	-2	-2	110
0	-2	00	110	-2	-2	110
-1	-2	11	110	-3	-3	001

There are two steps involved in the carry-free addition. The first step generates an intermediate carry and sum from the addend and augend. The second step combines the intermediate sum of the current digit with the carry of the lower significant digit. To prevent carry from further rippling, we define two rules. The first rule states that the magnitude of the intermediate sum must be less than or equal to 2.





The second rule states that the magnitude of the carry must be less than or equal to 1. Consequently, the magnitude of the second step output cannot be greater than 3 which can be represented by a single-digit QSD number; hence no further carry is required. all possible input pairs of the addend and augend are considered.

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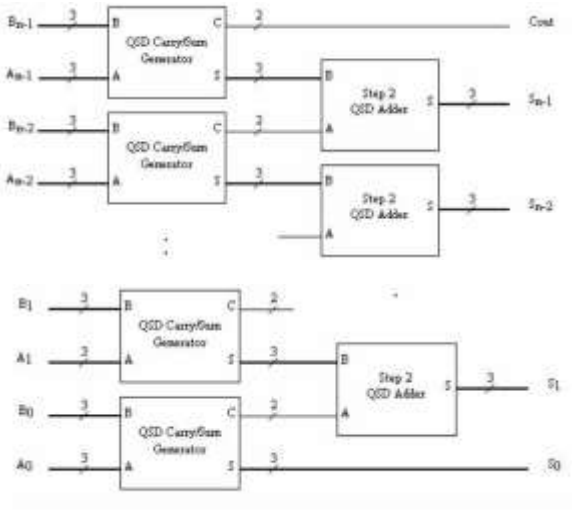

3. Multiplier Design

There are generally two methods for a multiplication operation: parallel and iterative. QSD multiplication can be implemented in both ways, requiring a QSD partial product generator and QSD adder as basic components. A partial product, Mi, is a result of multiplication between an n-digit input, An-1-A0, with a single digit input, Bi, where i = 0..n-1. The primitive component of the partial product generator is a single-digit multiplication unit whose functionality can be expressed .

Mult	QSD represented Number	QSD coding Number
-9	$2\ \bar{1},3\bar{3}$	$2\ \bar{1}$
-6	$2\bar{2},1\ 2$	$\bar{1}\ 2$
-4	$\bar{2}$	$\bar{1}0$
-3	$\bar{1}\ 1,0\bar{3}$	$1\ \bar{1}$
-2	$\bar{1}\ 2,0\bar{2}$	$0\bar{2}$
-1	$\bar{1}3,0$	$0\ \bar{1}$
0	00	00
1	01,13	01
2	02,12	02
3	03,1	$1\ \bar{1}$
4	10	10
6	12,22	12
9	21,33	21

The outputs of all possible combinations of a pair of multiplicand (A) andmultiplier (B).

A \ B	-3	-2	-1	0	1	2	3
-3	9	6	3	0	-3	-6	-9
-2	6	4	2	0	-2	-4	-6
-1	3	2	1	0	-1	-2	-3
0	0	0	0	0	0	0	0
1	-3	-2	-1	0	1	2	3
2	-6	-4	-2	0	2	4	6
3	-9	-6	-3	0	3	6	9

The single-digit multiplication produces M as a result and C as a carry to be combined with M of the next digit. The range of both outputs, M and C, is between -2 and 2. According to Table 8, and using the same procedure, the mapping between the 6-bit input, A and B, to the 6-bit output, M and C, results in six 6-varible Boolean expressions which represent a single-digit multiplication

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operation. The diagram of a single-digit QSD multiplier.

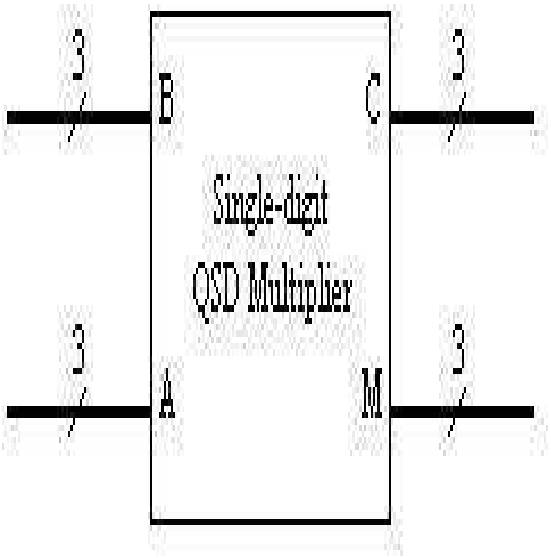

Figure 4. A single-digit QSD multiplier

The implementation of an n-digit partial product generator uses n units of the single-digit QSD multiplier. Gathering all the outputs to produce a partial product result presents a small challenge. The QSD representation of a single digit multiplication output contains a carry-out of magnitude 2 when the output is either -9 or 9. This prohibits the use of the QSD adder alone as a gatherer. In fact, we can use the complete QSD adder from the previous section as the gatherer. Furthermore, the intermediate carry and sum circuit can be optimized by not considering the input of magnitude 3. The QSD partial product generator implementation

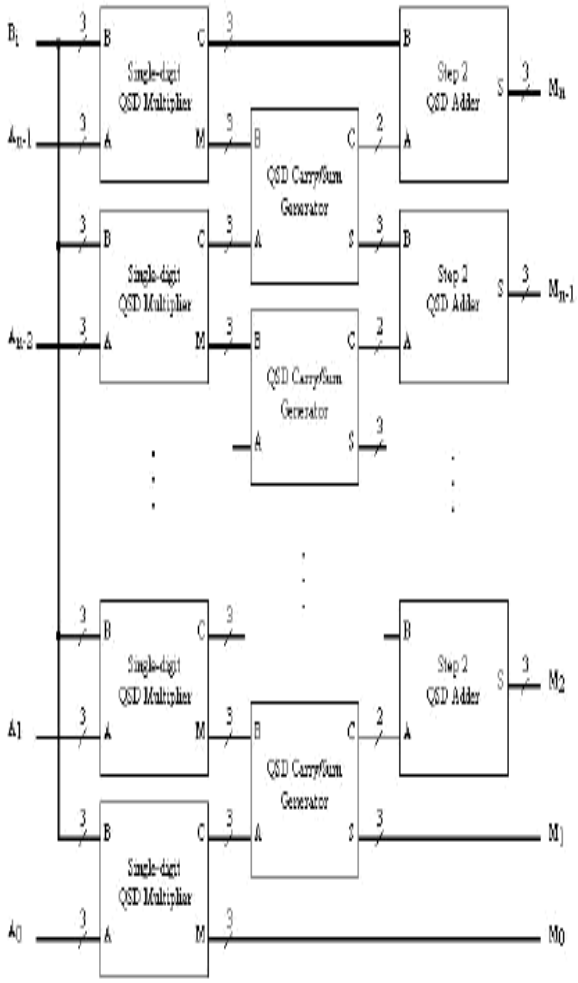

Figure 5. The *n*-digit QSD partial product generator.

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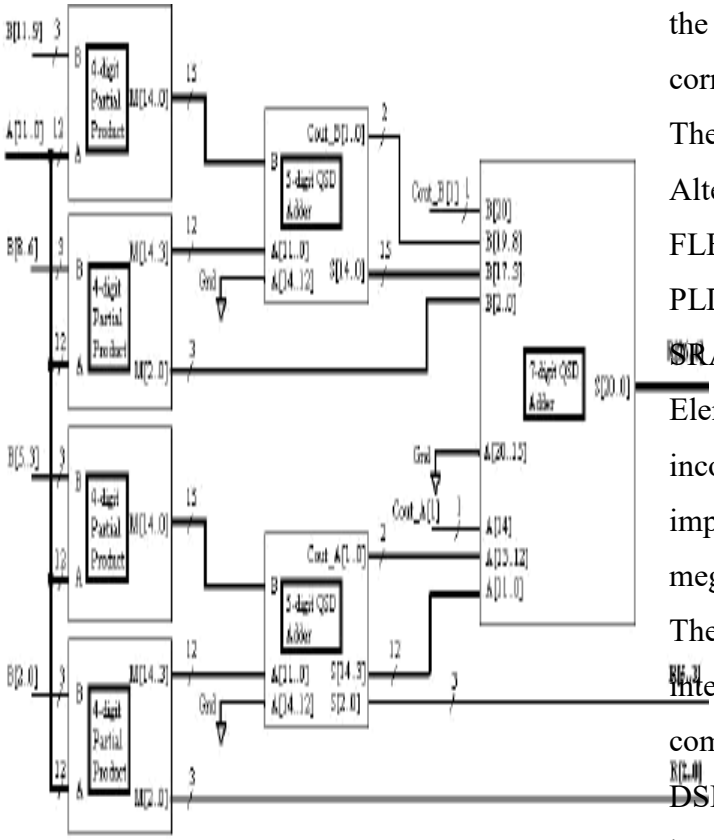

Figure 6. The 4x4 parallel QSD multiplication circuit

4. Results The QSD adder and multiplication circuit are written in VHDL and synthesized on Altera FPGA devices using LeonardoSpectrumtm from Mentor Graphics. The results of the implemented QSD addition and multiplication operations were collected from the timing simulation of the Altera MAX+plus II software. The correctness of the results is confirmed.

The device chosen for implementation is an Altera FLEX10K device. The Altera FLEX10K are the industry's first embedded PLDs. Based on reconfigurable CMOS SRAM elements, the Flexible Logic Element MatriX (FLEX) architecture incorporates all features necessary to implement common gate array megafunctions with up to 250,000 gates. The EPF10K70 device is ideal for intermediate to advanced design including computer architecture, communications, and DSP applications. The EPF10K70 device has over 70,000 typical gates, 3,744 Logic Elements (LEs), and 9 Embedded Array Blocks (EABs). We test the performance of the QSD adder against the binary ripple carry adder and the high performance Altera megafunction adder. The comparison of the registered performance . The test is performed for various sizes of the adder. The QSD number is capable of representing twice as much magnitude in each digit compared to the binary representation. Therefore, for an n-bit binary adder comparison, the n/2-bit QSD

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implementation is used for

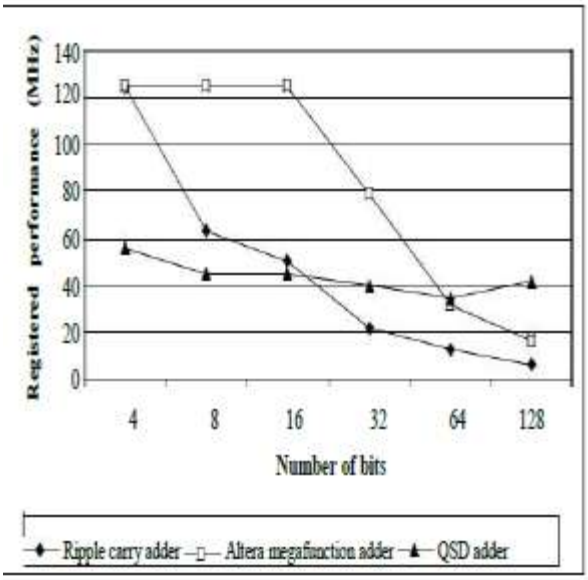

Figure 7. Comparison of the registered performance of all the test adders.

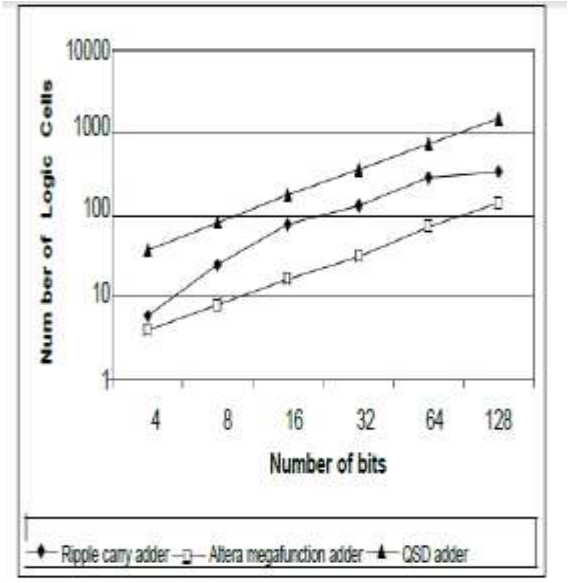

Figure 8. Comparison of the number of logic cells used in all the test adders.

5. Conclusions

The implementation of QSD addition and multiplication are presented. The test confirms the superior performance of the QSD adder implementation over other adders beyond 64-bits due to the carry-free addition scheme. The complexity of the QSD adder is linearly proportional to the number of bits which are of the same order as the simplest adder, the ripple carry adder. This QSD adder can be used as a building block for other arithmetic operations such as multiplication, division, square root, etc. With the QSD addition scheme, some well-known arithmetic algorithms can be directly implemented.

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ISSN: 2320-1363

International Journal of Trend in Research and Development, Volume 2(4), ISSN 2394-9333 www.ijtrd.com **IJTRD | July-August 2015 Available Online@www.ijtrd.com** 180 International Symposium on Circuits and Systems, pp 162-165, Vol. 4 , 2001.

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